TOSHIBA GTR Module Silicon N Channel IGBT

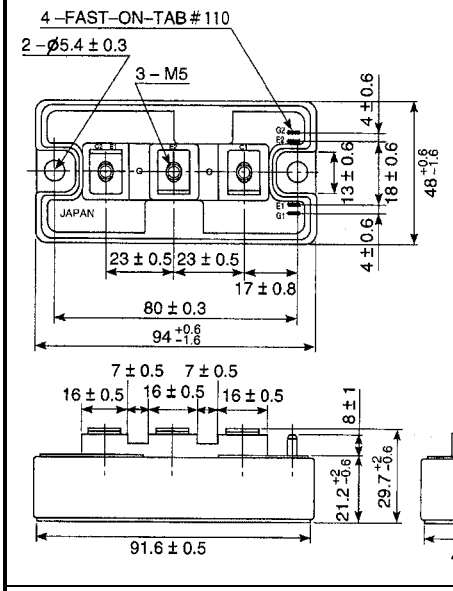
MG100Q2YS50

High Power Switching Applications

Motor Control Applications

- High input impedance
- High speed : t_f = 0.3μs (Max)
  @Inductive Load
- Low saturation voltage
  : $V_{CE\ (sat)}$ = 3.6V (Max)
- Enhancement-mode
- Includes a complete half bridge in one package.
- The electrodes are isolated from case.

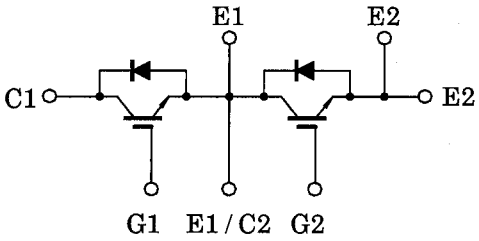
Unit: mm



JEDEC	—
EIAJ	—
TOSHIBA	2-95A4A

Weight: 255g

Equivalent Circuit



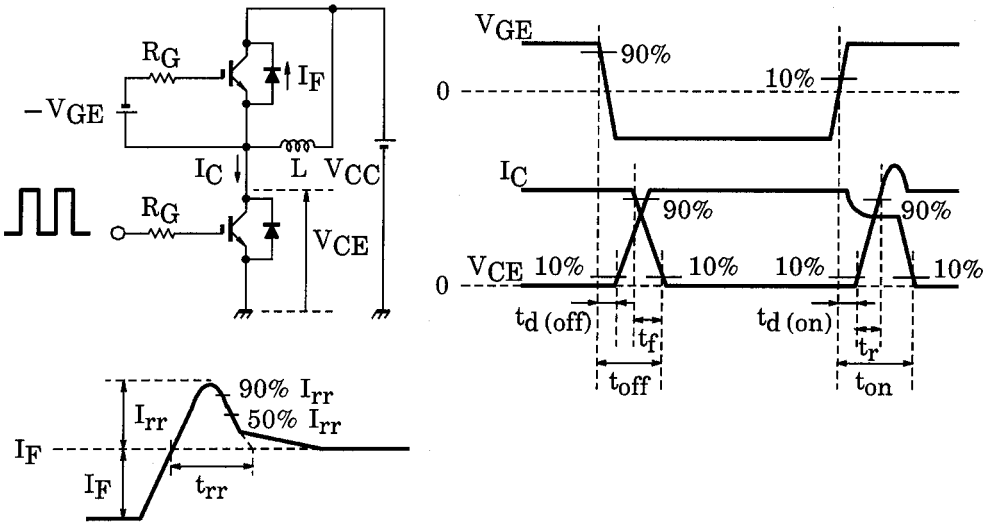
Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	1200	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current	DC	I_C (25°C / 80°C)	150 / 100	A
	1ms	I_{CP} (25°C / 80°C)	300 / 200	
Forward current	DC	I_F	100	A
	1ms	I_{FM}	200	
Collector power dissipation (Tc = 25°C)		P_C	660	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−40 ~ 125	°C
Isolation voltage		V_{Isol}	2500 (AC 1 min.)	V
Screw torque (Terminal / mounting)		—	3 / 3	N·m

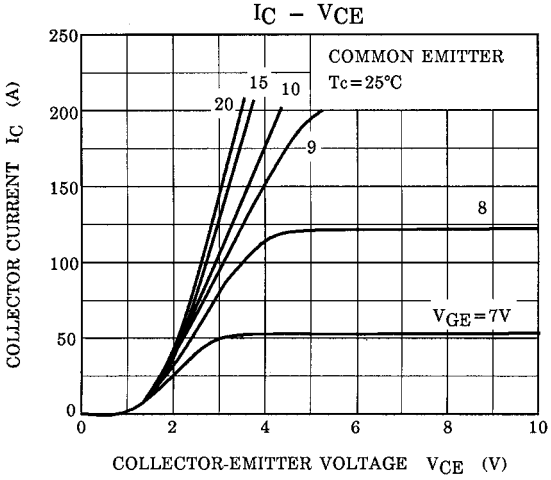
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition		Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±20V, V_{CE} = 0		—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 1200V, V_{GE} = 0		—	—	2.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (off)}$	I_C = 100mA, V_{CE} = 5V		3.0	—	6.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 100A, V_{GE} = 15V	T_j = 25°C	—	2.8	3.6	V
				T_j = 125°C	—	3.1	4.0	
Input capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz		—	12.0	—	nF
Switching time	Turn-on delay time	$t_{d(on)}$	Inductive load V_{CC} = 600V I_C = 100A V_{GE} = ±15V R_G = 9.1Ω (Note 1)		—	0.05	—	μs
	Rise time	t_r			—	0.05	—	
	Turn-on time	t_{on}			—	0.2	—	
	Turn-off delay time	$t_{d(off)}$			—	0.5	—	
	Fall time	t_f			—	0.1	0.3	
	Turn-off time	t_{off}			—	0.6	—	
Forward voltage		V_F	I_F = 100A, V_{GE} = 0		—	2.4	3.5	V
Reverse recovery time		t_{rr}	I_F = 100A, V_{GE} = −10V di / dt = 700A / μs (Note 1)		—	0.1	0.25	μs
Thermal resistance		$R_{th\ (j-c)}$	Transistor stage		—	—	0.16	°C / W
			Diode stage		—	—	0.47	

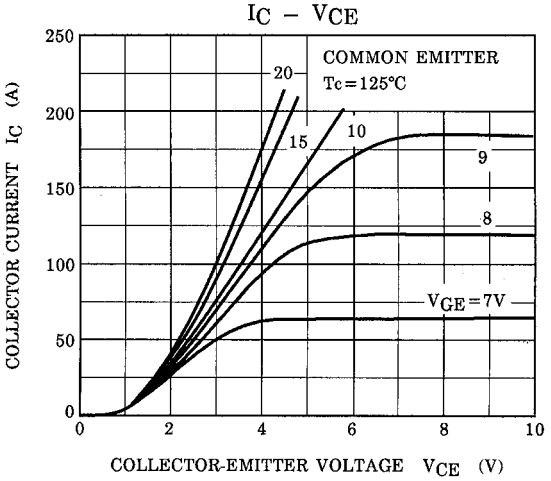
Note 1: Switching time and reverse recovery time test circuit & timing chart



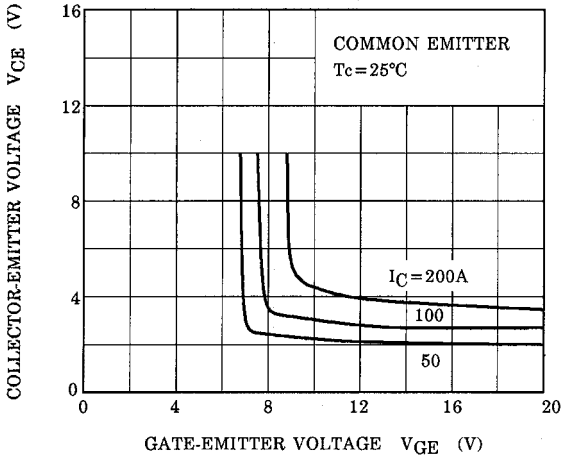
I_C – V_{CE}



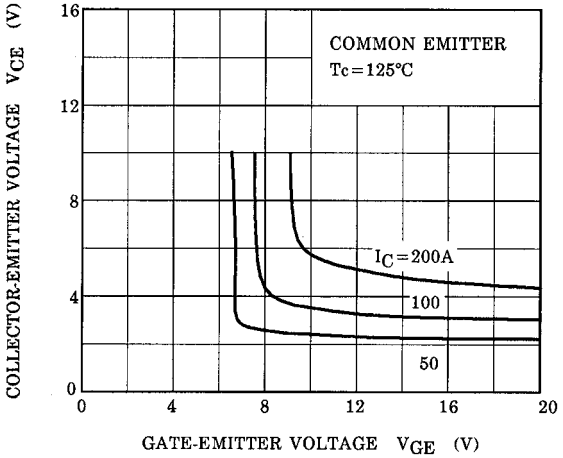
I_C – V_{CE}



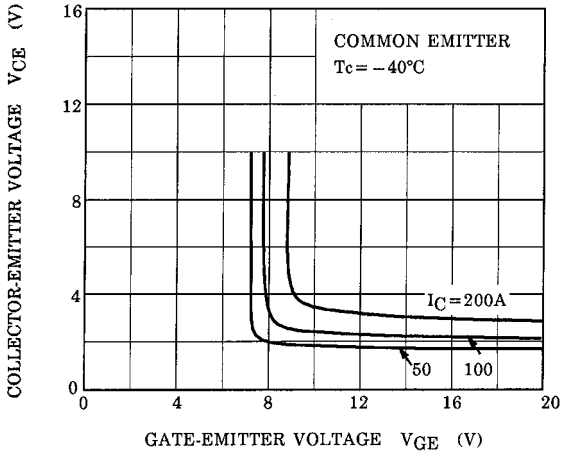
V_{CE} – V_{GE}



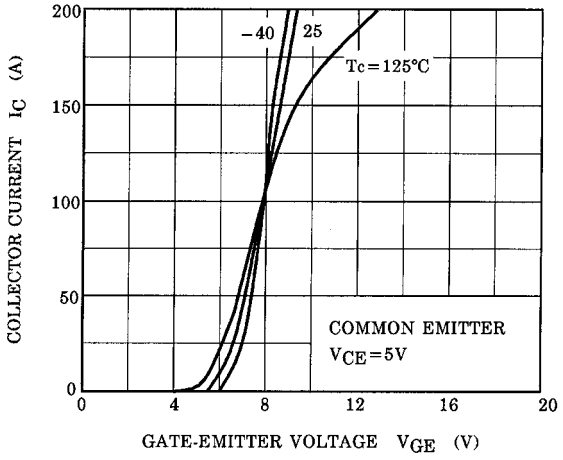
V_{CE} – V_{GE}



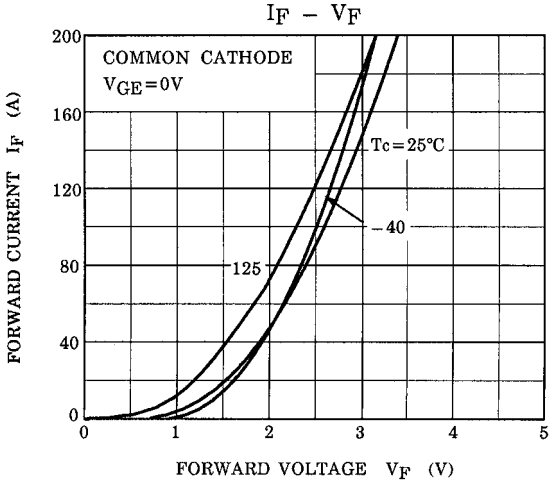
V_{CE} – V_{GE}



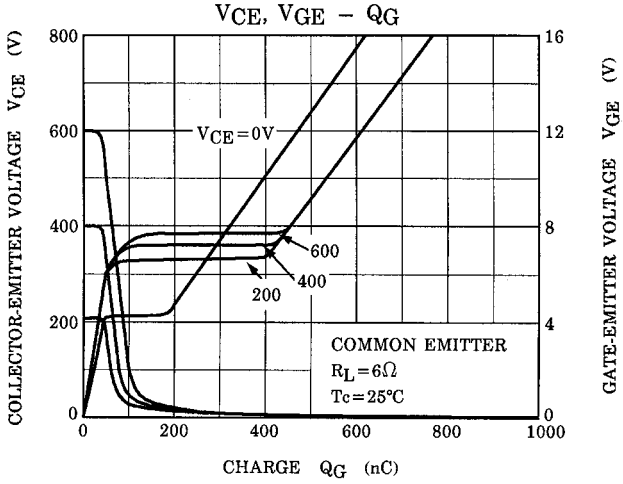
I_C – V_{GE}



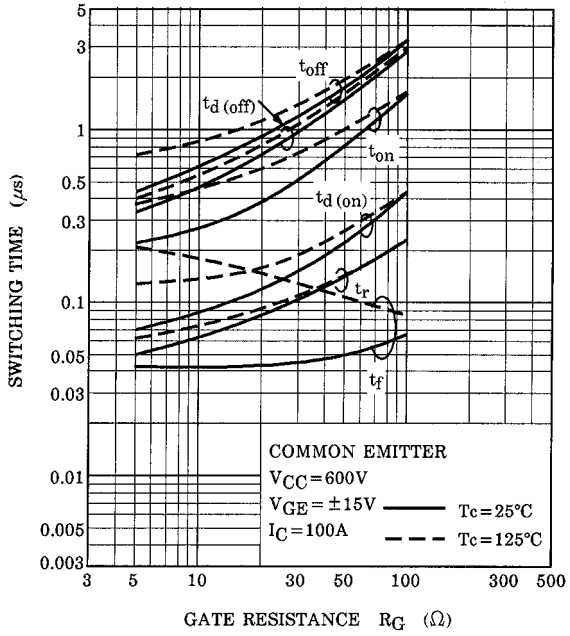
I_F – V_F



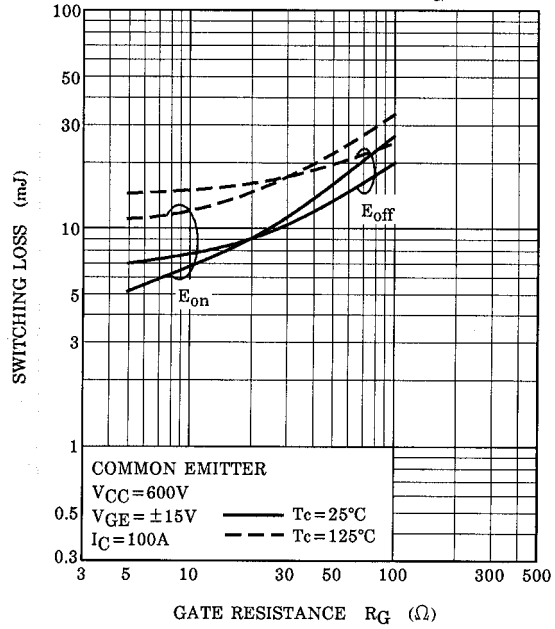
V_{CE}, V_{GE} – Q_G



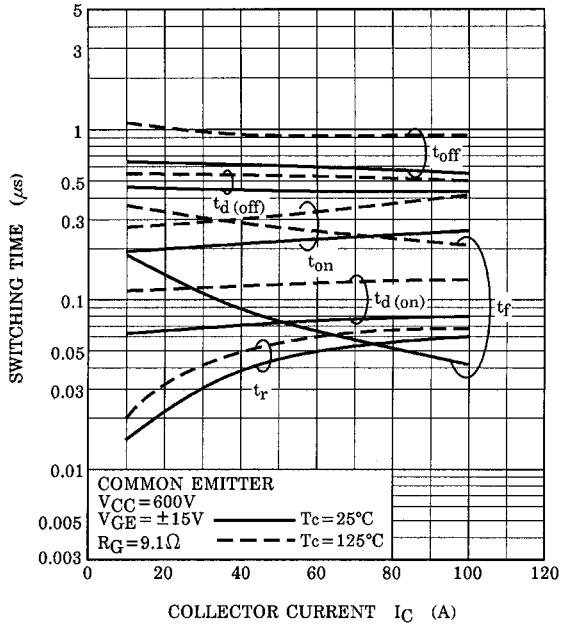
SWITCHING TIME – R_G



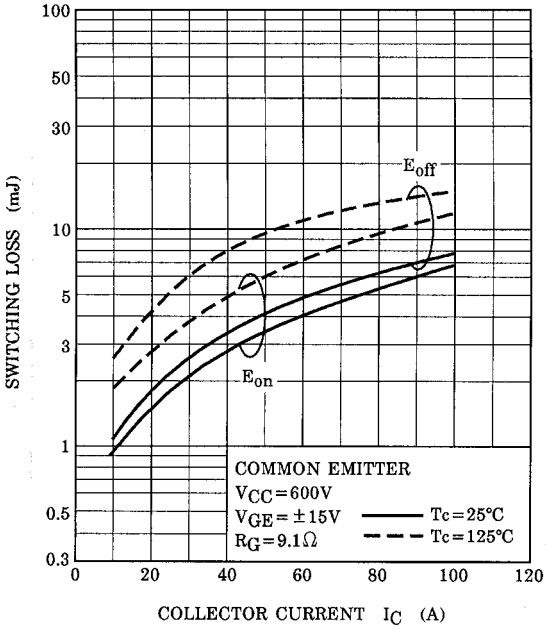
SWITCHING LOSS – R_G



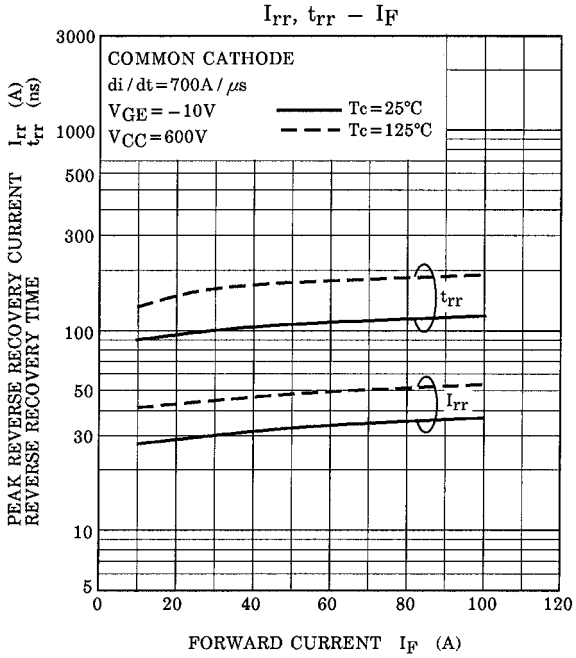
SWITCHING TIME – I_C



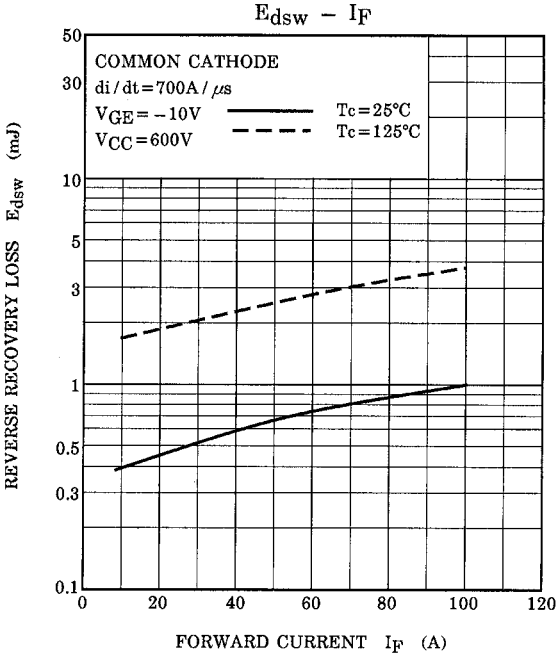
SWITCHING LOSS – I_C



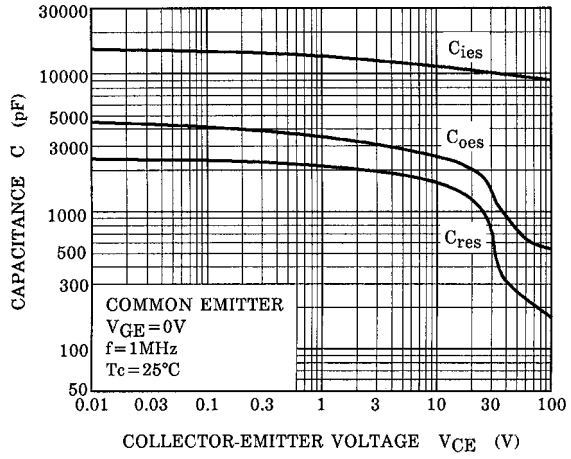
I_{rr}, t_{rr} – I_F



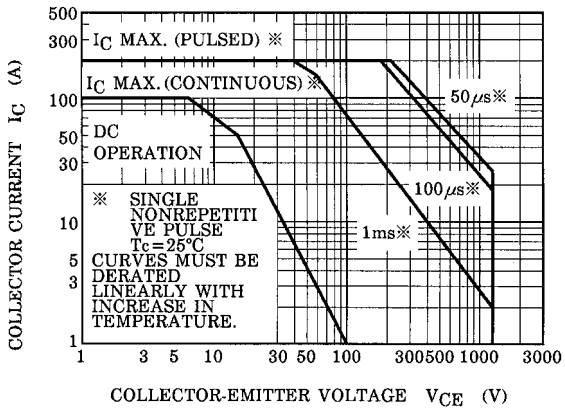
E_{dsw} – I_F



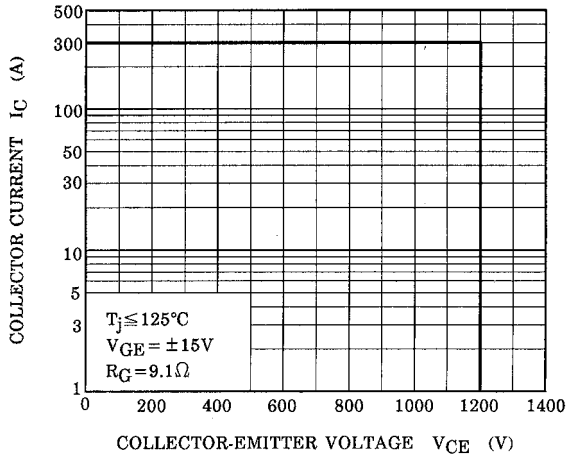
C – V_{CE}



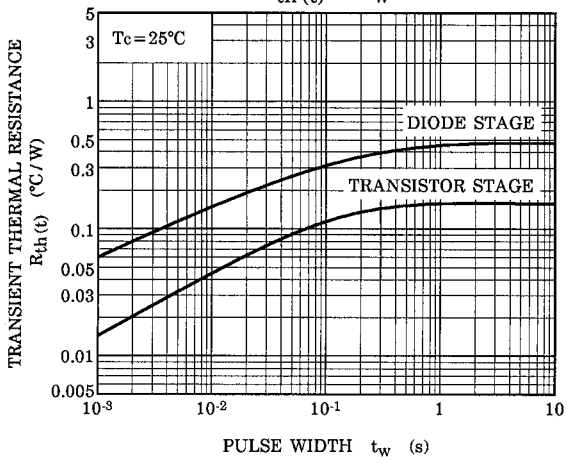
SAFE-OPERATING AREA



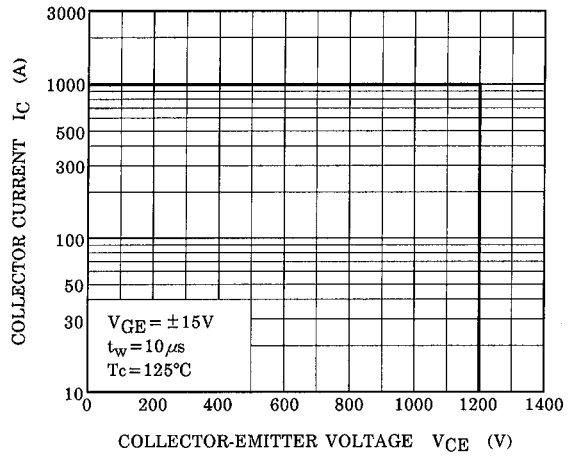
REVERSE BIAS SOA



R_{th} (t) – t_w



SHORT CIRCUIT SOA



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